Pspice Analysis of Parallel Operation of Two IGBT Inverters

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Abstract — Two full-bridge inverters are connected in parallel in order to increase power of a programmable AC source. Lossless current sharing by adding balancing inductors was investigated. Effects of IGBT parameter tolerances and temperature variations were analysed through ORCAD 9.2 PSPICE (including Monte Carlo analysis). It was found that manufacturing tolerances of balancing inductors have greater effect on the current sharing than IGBT parameter variations. Adding the inductors in series with both power rails, positive and negative, of the bridges reduces required inductance and improves current sharing. Results of the analysis will be used to build an experimental circuit.

Keywords — Programmable AC Source, Current Sharing, Inverter Bridge.

I. INTRODUCTION

Current Sharing Analysis of Parallel operation of two H-Bridges in ADC Accessory are represented in this paper. Main goal of this analysis was to improved manufacturing efficiency by increasing power of the power electronics equipment (used in the magnetron sputtering applications for thin film deposition of semiconducting materials).

II. REQUIREMENTS

The existing system consists of a standard high power DC source followed by a full bridge inverter**.** The inverter is capable of generating unipolar and bipolar pulses of various frequencies and duty cycles. An example of unipolar and bipolar outputs is shown in Fig. 1.

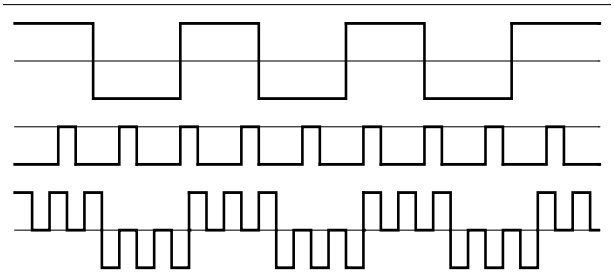

Fig. 1. Examples of output waveforms

Output power can exceed 10kW, with very wide, process dictated, ranges of output voltage and current – up to 1700V and 300A. Frequencies of interest are in a very wide range of 50Hz to 25kHz. A dedicated digital circuit is used to control the output in response to the system requirements.

In order to increase power, while avoiding major redesign and introducing risk to the established manufacturing process, it was decided to parallel two inverter stages. Requirement for current sharing was determined to be within 15%, not a very strict requirement. Due to the complexities of digital control and utilized digital feedback loop compensation, standard current sharing schemes were not deemed practical, due to the implications on project timing and risk assessment. It was decided that a simpler approach is analyzed – a possibility of driving both inverters with identical drive signals and adding series inductors in line with the two paralleled inverters. Sensitivity analysis to temperature changes (affecting IGBT parameters), inductance values and tolerances and, finally, sensitivity to combined effects was the critical part of the project.

III. SIMULATION MODEL

Initial circuit, as modeled in PSpice is shown in Fig. 2. The model includes some of the relevant parasitic elements, values of which were estimated based on the existing inverters.

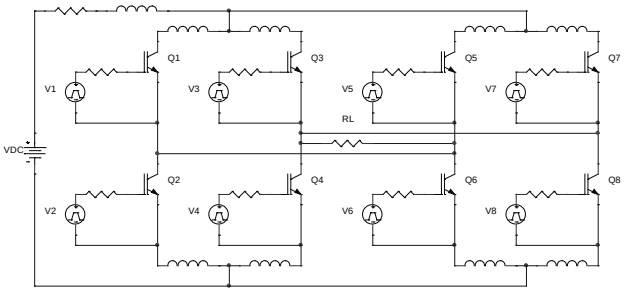

Fig.2. Initial simulation model

IGBT parameters suitable for PSpice simulation model are listed in Table I. The two bridges use IGBT modules SEMIKRON SKM400GB176D.The modules are built based on INFINEON part number SIGC186T170R3. After longer research and communication with INFINEON's applications engineers it was found that adequate replacement, for which simulation models are available is EUPEC's (formerly SIEMENS and now acquired by INFINEON) part number BSM150GB100D.

After running Monte Carlo analysis and varying for IGBT parameters and operating temperatures, the obtained results were expectedly poor, as shown in Table II. For brevity, results for only two switches, in identical positions, are shown. Simulated load current is 200A.

As we are using computer-generated random numbers for the analysis (the random number seed), it is important to note that, in reality, these are pseudorandom numbers, due to the deterministic nature of the computers. If the seed number is repeated, identical random numbers will be repeated as well. For multiple trials, different random number seeds were used, as presented in the Table II.

The Table II lists only the worst case current through the switch for each set of simulations. Highlighted are the worst case deviations. Ideally, current through each IGBT would have been 100A – large deviations from the ideal

number prove the need for forced current sharing.

TABLE I.
IGBT MODEL PARAMETERS

Model Parameters	**Symbol**	**Value**
AREA (area of the device)	A	1.858 cm2
AGD (gate-drain overlap area)	A_{GD}	1.4823 cm2
KP (MOS transconductance)	K_p	3.54 A/V2
KF (triode region factor)	K_f	
CGS (gate-source capacitance per unit area)	C_{GS}	10.7 nF/cm2
COXD (gate-drain oxide capacitance per unit area)	C_{OXD}	59.3 nF/cm2
VT (threshold voltage)	V_T	5.8
TAU (ambipolar recombination lifetime)	T	$8x10^{-6}$ cm
WB (metallurgical base width)	W_B	$36.7385x10^{-3}$ cm
NB (base doping)	N_B	$0.1651x10^{14}/cm^3$

TABLE II
CURRENT SHARING OF THE ORIGINAL CIRCUIT

No.	Seed number	ICQ2 (A)		ICQ6 (A)	
		min.	max.	min.	max.
1	default	86.5	130.1	68.7	109.1
2	100	109.5	122.7	76.2	89.5
3	1000	92.6	126.4	72.5	101.1

Figure 3 shows four current sharing inductors added to each leg of both paralleled inverters. The results for added 10μH inductance are summarized in Table III. The inductance was selected based on the excellent results (5% deviations) when temperature effects on IGBT parameters are neglected.

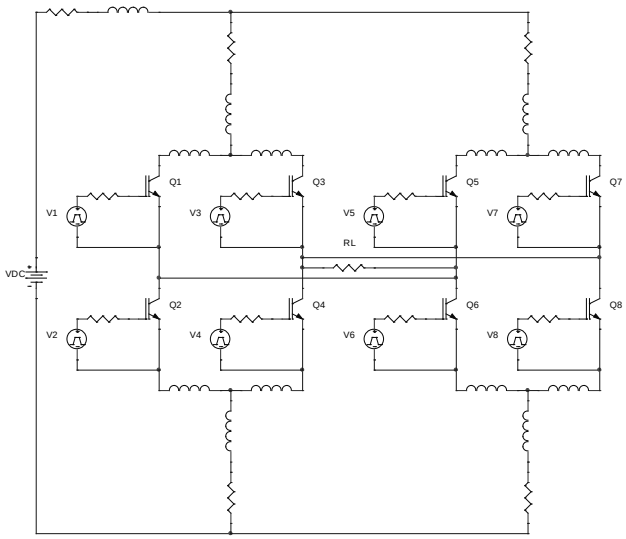

Fig. 3. Model with current sharing inductors

TABLE III
CURRENT SHARING WITH 10μH BALANCING INDUCTORS

No.	Seed number	ICQ2 (A)		ICQ6 (A)	
		min.	max.	min.	max.
1	default	102.6	126.5	88.4	96.2
2	10000	102.3	120.6	78.1	96.5
3	30000	107.7	124.7	74.1	91.2

The results indicate that, when IGBT parameters are taken into account, achieved results are modest, at best.

IV. VARIATIONS OF KEY PARAMETERS

It is obvious that seed number also plays significant role in the final outcome. Of course, this is little related to the actual operation of the circuit and warrants a closer look. Table IV summarizes I_{CQ2}-I_{CQ6} values for different seed numbers.

TABLE IV
DEPENDENCE OF CURRENT IMBALANCE ON SELECTED SEED NUMBER

Seed number	I_{CQ2}-I_{CQ6} (A), max.	
	No inductors	10uH inductors,
default	61.24	22.14
10	41.91	28.08
100	46.57	33.78
1000	31.6	27.05
10050	48.18	**36.50**

It is interesting to note that selected seed number has much larger effect on the circuit without balancing inductors then on the one with 10uH inductors. Relative to the load current of 200A, worst case imbalance is 36.5A, or 18.2%.

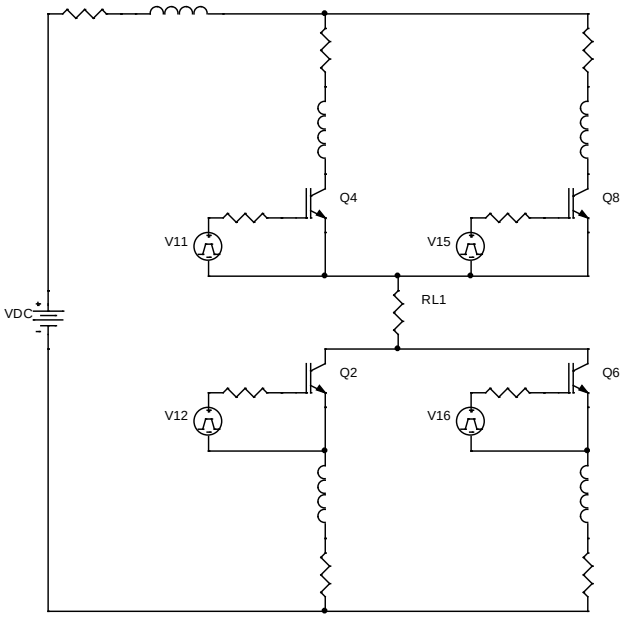

Fig. 4. Simplified circuit

So far, adding balancing inductors to decouple the two inverter bridges did not result in significant improvements. Further improvements were investigated. It was found that adding balancing inductors in series with emitters of the IGBTs with grounded emitters (low

side switches Q2, Q6, Q3 and Q7) has significant effects. Rather than running the initial model (Fig. 1) and change inductor values, the schematic was simplified in order to minimize convergence errors. Only IGBTs connected in parallel are shown. The simplified circuit is shown in Fig. 4 and summary results in Table V.

TABLE V
CURRENT SHARING WITH BALANCING EMITTER INDUCTORS

Added inductance	ICQ2 (A)	ICQ6 (A)
1uH	111.4	87.5
5uH	108.4	90.5
10uH	**105.6**	**93.2**
20uH	103.2	95.8

The table outlines worst case results of several simulations with different inductance values and seed numbers. Upon examination of results, and comparison with those shown in Tables III and IV, improvements are significant, deviation from ideal current sharing is less than 7%. It is interesting to note that adding the same inductor values into the collector circuits does not yield any improvements.

One example of simulation resulsts are given in Figure 5. econg example can be seen in Figure 6 (illustrates simulation results ICQ2-ICQ6 for L3=L4=L5=L6=10uH and Iload=50A).

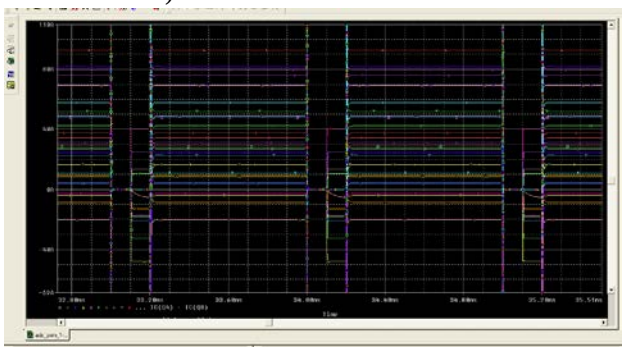

Figure 5: Differences in collector currents between Q4 and Q8

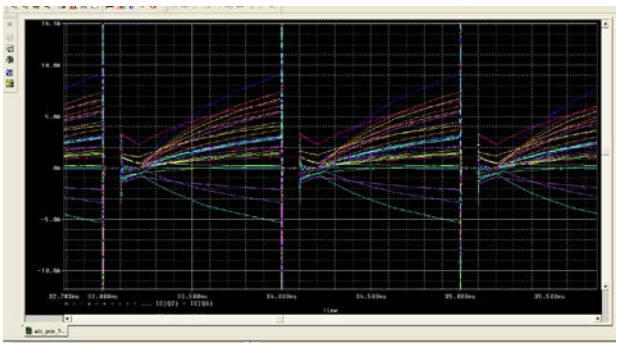

Figure 6: Differences in collector currents between Q2 and Q6

V. INDUCTOR TOLERANCES

The paper further discusses analyses for various duty cycles and load currents, finding and addressing the worst case scenario. Final inductance value of 70uH is identified as acceptable, and analyzed for the manufacturing tolerances.

Table VI summarizes worst case analysis, combining effects of IGBT parameter variations and inductor tolerances.

TABLE VI
CURRENT SHARING RELATIVE TO 70UH INDUCTOR TOLERANCES

	20%	10%	5%	3%	1%
I_{CQ2avg}/ I_{CQ6avg}	1.45	1.22	1.13	1.11	1.08
I_{CQ4avg}/ I_{CQ8avg}	1.33	1.17	1.12	1.09	1.07

Here we are looking at ratio of currents through IGBT's in identical positions. 5% tolerance allows meeting the requirement for current sharing within 15%.

VI. PRACTICAL OBSERVATIONS

Based on the previous analyses the following observations can be made:

1. The very basic current balancing scheme with one balancing inductor per H-bridge was evaluated against somewhat more complex scheme using two inductors per bridge, one in the upper leg and one in the lower leg of each paralleled bridge. The latter was proved to be more effective and results in significantly smaller required inductance

2. Variations of IGBT parameters have much lesser effects than balancing inductor tolerances.

3. Tolerances of the balancing inductors should be within ±5% (from each other) in order to ensure current sharing within 15%.

4. It is desired to have IGBT parameters vary within 10% (DEV=10% and LOT=5%). This combined with inductor tolerances of DEV=10% results in adequate current sharing. It proved difficult to obtain exact parameter distributions from component vendors and it may be impossible to establish any type of control over the parameters, however, manufacturer's applications engineers feel that normal distribution falls well within the desired tolerances.

5. Inductor values of 70uH are adequate for switching frequencies of fs≥1kHz. For low switching frequencies inductor values need to increase (inversely proportional increase seems like a reasonable approximation).

6. It is important to reiterate that

a. Simulations did not take into account positive temperature coefficient of chosen IGBTs. It was assumed that there is a fixed difference in Vces due to temperature differences: this is the worst case and in practical circuit Vces of the two IGBTs operating at different temperatures will tend to drift toward each other minimizing the difference and improving current sharing.

b. Snubber circuits were not simulated due to convergence problems. Resulting reduction in current rise time (di/dt) is neglected, which again results in somewhat worse current sharing than could be expected in a practical circuit.

c. Analyses were performed with duty cycle of D=0.8 and D=0.1. Presented results are given for the worse of the two cases (constant D=0.8), which again may lead to somewhat exaggerated imbalances.

7. In summary, the proposed current balancing scheme uses two inductors, one in the upper and one in the lower leg of the H-bridge. Target current sharing can be achieved by using reasonable inductance of 70uH, assuming IGBT parameter values variations of 10% or less and inductor tolerance of ≤5%.

VI. CONCLUSION

In order to achieve significant increase in output power of the high power programmable waveform AC source, without major redesign effort, it was decided to connect two inverter bridge circuit in parallel. Given sufficient power reserve, current sharing requirements were set at 15% over the range of output loads.

Computer simulation and Monte Carlo analysis was used to determine the worst case operating conditions and determine minimum required inductance value and tolerance.

The basic lossless current sharing scheme, by using one inductor per inverter bridge was compared with the concept using two inductors, one in positive and the other one in negative leg of each paralleled bridge. The latter was proved to be more effective requiring significantly smaller required inductance. Adding inductors in series with IGBT emitters further improves current sharing, albeit at added cost and complexity.

Variations of IGBT parameters have less effect on the current sharing than tolerances of added inductors. Tolerance of ±5% is sufficient to allow current sharing within 15%.

An experimental circuit is currently being built for laboratory and field evaluations.

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